

Govt. Women Engineering College, Ajmer

Department of Computer Science and Engineering

B. Tech V Semester IInd Mid Term Examination – November 2017

Subject: Computer Architecture Subject Code: 5CS1

Time: 1 Hr.

Max. Marks: 20

Date of Examination: 7/11/2017

- Q. 1** Design the algorithm to implement the operations Addition and Subtraction for signed magnitude data. 7
OR
- Q. 2** Discuss about the restoring method to calculate division operation. 7
- Q. 3** Explain the virtual memory system. 5
- Q. 4** How Booth multiplication algo is different from general multiplication algo. 3
- Q. 5** Write short note on any one : (a) Direct associative cache memory
(b) Set associative cache memory 5

Govt. Women Engineering College, Ajmer

Department of Computer Science and Engineering

B. Tech V Semester IInd Mid Term Examination – November 2017

Subject: Computer Architecture Subject Code: 5CS1

Time: 1 Hr.

Max. Marks: 20

Date of Examination: 7/11/2017

- Q. 1** Design the algorithm to implement the operations Addition and Subtraction for signed magnitude data. 7
OR
- Q. 2** Discuss about the restoring method to calculate division operation. 7
- Q. 3** Explain the virtual memory system. 5
- Q. 4** How Booth multiplication algo is different from general multiplication algo. 3
- Q. 5** Write short note on any one : (a) Direct associative cache memory
(b) Set associative cache memory 5

Govt. Women Engineering College, Ajmer

Department of Computer Science and Engineering

B. Tech V Semester IInd Mid Term Examination – November 2017

Subject: Computer Architecture Subject Code: 5CS1

Time: 1 Hr.

Max. Marks: 20

Date of Examination: 7/11/2017

- Q. 1** Design the algorithm to implement the operations Addition and Subtraction for signed magnitude data. 7
OR
- Q. 2** Discuss about the restoring method to calculate division operation. 7
- Q. 3** Explain the virtual memory system. 5
- Q. 4** How Booth multiplication algo is different from general multiplication algo. 3
- Q. 5** Write short note on any one : (a) Direct associative cache memory
(b) Set associative cache memory 5

Govt. Women Engineering College, Ajmer

Department of Computer Science and Engineering

B. Tech V Semester IInd Mid Term Examination – November 2017

Subject: Computer Architecture Subject Code: 5CS1

Time: 1 Hr.

Max. Marks: 20

Date of Examination: 7/11/2017

- Q. 1** Design the algorithm to implement the operations Addition and Subtraction for signed magnitude data. 7
OR
- Q. 2** Discuss about the restoring method to calculate division operation. 7
- Q. 3** Explain the virtual memory system. 5
- Q. 4** How Booth multiplication algo is different from general multiplication algo. 3
- Q. 5** Write short note on any one : (a) Direct associative cache memory
(b) Set associative cache memory 5

