

Govt. Women Engineering College, Ajmer

All the Best

Department of Computer Science and Engineering

A

B. Tech V Semester I Mid Term Examination – September 2017

Subject: CA

Subject Code: 5CS1

Time: 1 Hr.

Max. Marks: 20

Date of Examination: 18/09/2017

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- Q. 1** Discuss, RISC vs. CISC [5]
- Q. 2** A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec respectively. The delay of latches (buffer between two stages) is 0.5 nsec. The speedup of pipelined processor for a large number of instructions is. [3]
- Q. 3** Discuss Shift Micro Operations with diagram and example. [3]
- Q. 4** Draw the block diagram of the hardware that implements the following statement. [4]
- $$xyT_0 + T_1 + y'T_2 : AR \leftarrow AR + BR$$
- Q. 5** Construct a common bus system by Three-state buffer gate for 4 Register each of which having 4 bits. And consider a common bus constructed by multiplexer for 16 registers of 32 bit each. Then, how many multiplexer are required and what is the size of each multiplex. [5]

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B

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- Q. 1** Show that the theoretical maximum speedup that a pipeline can provide is equal to the number of segments in the pipeline. [5]
- Q. 2** Illustrate the influence of the number of addresses on computer program for the arithmetic expression $X = (A+B) \times (C+D)$ using Zero, One, Two and Three Address instruction with the advantages and disadvantages of each. [5]
- Q. 3** Design a 4-bit combinational circuit of decremter by using four full-adder circuits [3]
- Q. 4** Explain the Register Transfer of Fetch and Decode phase in Instruction Cycle with respect to timing signals. [4]
- Q. 5** Discuss the Flynn Classifications [3]

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C

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- Q. 1** Discuss the instruction pipeline for the instruction cycle that is divided into four segments of equal duration with handling of branch type instructions. [5]
- Q. 2** Explain Addressing Modes in details with suitable example and diagrams. [5]
- Q. 3** Draw the block diagram of Common bus of 4 Registers of 8 bit each. [4]
- Q. 4** Show the block diagram of the hardware that implements the following register transfer statement. If $(P=1)$ then $(R_1 \leftarrow R_2)$ else if $(Q=1)$ then $(R_1 \leftarrow R_3)$ [4]
- Q. 5** Discuss the Von-Neumann [2]