Q. 1 Discuss, RISC vs. CISC

Q. 2 A non pipelined single cycle processor operating at 100 MHZ is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec respectively. The delay of latches (buffer between two stages) is 0.5 nsec. The speedup of pipelined processor for a large number of instructions is.

Q. 3 Discuss Shift Micro Operations with diagram and example.

Q. 4 Draw the block diagram of the hardware that implements the following statement.

\[ xyT_0 + T_1 + y'T_2 : AR \leftarrow AR + BR \]

Q. 5 Construct a common bus system by Three-state buffer gate for 4 Register each of which having 4 bits. And consider a common bus constructed by multiplexer for 16 registers of 32 bit each. Then, how many multiplexer are required and what is the size of each multiplexer.

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Q. 1 Show that the theoretical maximum speedup that a pipeline can provide is equal to the number of segments in the pipeline.

Q. 2 Illustrate the influence of the number of addresses on computer program for the arithmetic expression \( X = (A+B) \times (C+D) \) using Zero, One, Two and Three Address instruction with the advantages and disadvantages of each.

Q. 3 Design a 4-bit combinational circuit of decrementer by using four full-adder circuits

Q. 4 Explain the Register Transfer of Fetch and Decode phase in Instruction Cycle with respect to timing signals.

Q. 5 Discuss the Flynn Classifications